CLAIMS

What is claimed is:

1. A device for associating indexes to addresses chosen from among a greater number of values than the number of available indexes, including:

a memory containing indexes and respective check words corresponding to predetermined bits of the addresses associated with the indexes;

a packing circuit receiving a current address and suppressing in this address bits determined by a pattern such that the suppressed bits correspond to bits of the check words, the packed address provided by the packing circuit being used to select in the read mode a memory location; and

a comparator indicating that the current address corresponds to the selected memory location if the bits of the check word of the selected location are equal to the corresponding bits of the current address.

2. The device of claim 1, wherein the device includes a mask circuit which, according a predetermined mask, annuls bits other than those suppressed by the packing circuit, which also correspond to check word bits.

3. The device of claim 1, wherein each memory location contains an enable bit indicating whether the location is occupied or not.

4. The device of claim 1, wherein the addresses are ATM network addresses, and the indexes identify connections of the device to one or several ATM networks.

5. The device of claim 4, wherein the addresses provided by the packing circuit have a 16-bit size, the indexes have a 10-bit size, and the check words correspond to the 20 most significant bits of the ATM addresses.

6. The device of claim 5, further comprising an input configured to be connected to 16 ATM networks, the addresses provided to the device having 4 most significant bits enabling identification of the corresponding ATM networks.

7. An address association device, comprising:

a masking circuit configured to receive a plurality of address bits and mask the address bits in accordance with a predetermined mask pattern;

a packing circuit configured to receive address bits from the masking circuit and to reduce the number of address bits to a plurality of index bits and a plurality of check word bits according to a predetermined packing pattern;

a memory configured to receive from the packing circuit the plurality of index bits and the plurality of check word bits and to associate the received index bits and check word bits with the memory location of a network connection; and

a comparator coupled to the memory and configured to receive the plurality of address bits and to indicate if selected bits from the plurality of address bits correspond to the plurality of check word bits associated with the memory location addressed in the plurality of address bits.

8. The device of claim 7 wherein the masking circuit is configured by the predetermined mask pattern to mask bits not suppressed by the packing circuit when the number of bits used to address a network connection in memory is fewer than the number of bits remaining after the plurality of address bits are reduced by the packing circuit.

9. The device of claim 7 wherein each network connection in memory includes an enable bit that is configured to signal when the network connection in memory is an active connection to the network.

10. The device of claim 9, further comprising a logic circuit coupled to the enable bit and to the comparator and configured to indicate if a selected location addressed by the plurality of address bits is an active location.

11. The circuit of claim 7, further comprising a register configured to store a base address corresponding to a beginning address in memory and, further comprising an adder for adding the base address to the plurality of address bits reduced by the packing circuit.

12. A method for associating addresses to memory locations, comprising:

receiving a plurality of address bits and masking the address bits in accordance with a predetermined mask pattern;

packing the masked plurality of address bits to reduce the number of address bits to a plurality of index bits and check word bits according to a predetermined packing pattern;

associating the plurality of index bits and check word bits with a memory location corresponding to a network connection; and

comparing selected bits from the plurality of address bits for a selected memory location with selected bits associated with a memory location addressed in the plurality of address bits and indicating if there is a match.

13. The method of claim 12 wherein masking comprises configuring the predetermined masking pattern to mask bits not suppressed by packing when the number of bits used to address a selected memory location is fewer than the bits remaining after packing.

14. The method of claim 12, further comprising ANDing an enable bit with the results of the comparing to determine if a selected memory location is an active connection.

15. The method of claim 12 wherein packing comprises storing a base address corresponding to a beginning address in memory and adding the base address to the plurality of address bits reduced during packing.

16. The method of claim 12 wherein packing further comprises reducing the plurality of address bits to a packed address comprising a plurality of index bits and check word bits used to select a memory location in a read mode.

17. The method of claim 14, further comprising disabling an enable bit corresponding to a memory location selected by the plurality of address bits.

18. The method of claim 17 wherein masking comprises configuring the predetermined mask pattern to mask bits not suppressed by packing when the number of bits used to address a selected memory location is fewer than the bits remaining after packing, and further comprising configuring the predetermined mask pattern to mask bits to prevent accessing selected memory locations that have been previously addressed.